ABSTRACT

The object of this invention is to provide a distributed memory type computer architecture that can achieve extremely high speed parallel processing. The computer system 10 comprises: a CPU module 12, a plurality of memory modules 14, each of which having a processor 36 and RAM core 34, and a plurality of sets of buses 24 that make connections between the CPU and the memory modules and/or connections among memory modules, so that the various memory modules operate on an instruction given by the CPU. A series of data having a stipulated relationship is given a space ID and each memory module manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data, and, the processor of each memory module determines if the portion of the series of data that it manages itself is involved in a received instruction and performs processing on data stored in the RAM core.